Amendments to the Claims

Please amend claims 8 and 12 such that the pending claims will read as follows:

1. (Original) A memory system comprising:

a scalable termination circuit having:

a first resistive element coupled to a first port;

a second resistive element coupled to a second port;

a first logic circuit coupled to the first and second resistive elements, and adapted to determine a characteristic impedance of the first port by generating a plurality of binary termination signals; and

a second logic circuit coupled to the first logic circuit and the second resistive element, and adapted to modify a characteristic impedance of the second port by manipulating one or more of the plurality of binary termination signals.

2. (Original) The memory system of claim 1 further comprising a third logic circuit coupled to the second resistive element, and adapted to modify the characteristic impedance of the second port by outputting control signals to the second resistive element.

3. (Original) The memory system of claim 2 wherein each of the first and second resistive elements includes a plurality of stacked transistor pairs connected in parallel; and wherein each of the first and second resistive elements includes a default device that is always

on, the default device includes a plurality of stacked transistors connected in parallel.

4. (Original) The memory system of claim 3 wherein the third logic circuit is further adapted to modify the characteristic impedance of the second port by outputting control signals to one of the plurality of stacked transistor pairs included in the default device of the second resistive element.

5. (Original) The memory system of claim 1 wherein the second logic circuit is further adapted to modify the characteristic impedance of the second port by manipulating one or more of the plurality of binary termination signals by performing at least one of a multiplication and division operation on the binary termination signals.

6. (Original) The memory system of claim 1 wherein each of the first and second resistive elements includes a plurality of stacked transistor pairs connected in parallel.

7. (Original) The memory system of claim 6 wherein each of the first and second resistive elements includes a default device that is always on, the default device includes one or more stacked transistor pairs connected in parallel.

8. (Currently Amended) A method of providing multiple termination values using a plurality of binary termination signals comprising:

determining a characteristic impedance of a first port by generating a plurality of binary termination signals at a first logic circuit; and

modifying a characteristic impedance of a second port by manipulating one or more of the plurality of binary termination signals at a second logic circuit.

9. (Original) The method of claim 8 wherein modifying the characteristic impedance of the second port includes modifying the characteristic impedance of the second port by manipulating one or more of the plurality of binary termination signals by performing at least one of a multiplication and division operation.

10. (Original) The method of claim 8 further comprising modifying the characteristic impedance of the second port by outputting control signals to a resistive element coupled to the second port.

11. (Original) The method of claim 10 wherein modifying the characteristic impedance of the second port includes modifying the characteristic impedance of the second port by outputting control signals to one of a plurality of stacked transistor pairs included in a default device of the resistive element coupled to the second port.

12. (Currently Amended) A method of providing multiple termination values using a set of control signals comprising:

employing the set of control signals generated at a first logic circuit to provide a fixed output impedance on a first port; and

employing the set of control signals at a second logic circuit to provide a variable output impedance on a second port.

13. (Original) The method of claim 12 wherein employing the set of control signals to provide a variable output impedance on the second port includes:

if a first logic circuit is enabled, modifying one or more of the control signals using the first logic circuit thereby creating modified control signals; and

adjusting the output impedance on the second port using the modified control signals.

14. (Original) The method of claim 13 wherein adjusting the output impedance on the second port includes at least one of selectively activating and de-activating one or more of a plurality of stacked transistor pairs included in a resistive element coupled to the second port using the modified control signals.

15. (Original) The method of claim 13 further comprising:

if a second logic circuit is enabled, modifying one or more secondary control signals using the second logic circuit; and

adjusting the output impedance on the second port using the modified secondary control signals.

16. (Original) The method of claim 15 wherein adjusting the output impedance on the second port includes at least one of selectively activating and de-activating

one or more of a plurality of stacked transistor pairs included in a default device of a resistive element coupled to the second port using the modified secondary control signals.

17. (Original) A memory system comprising:

a scalable termination circuit having:

a first resistive element coupled to a first port;

a second resistive element coupled to a second port;

an impedance evaluation control circuit coupled to the first and second resistive elements and adapted to employ a set of control signals to provide a fixed output impedance on a first port; and

first termination adjustment logic coupled to the impedance evaluation circuit and the second resistive element, and adapted to employ the set of control signals to provide a variable output impedance on the second port.

18. (Original) The memory system of claim 17 wherein the first termination adjustment logic is further adapted to:

if the first termination adjustment logic is enabled, modify the set of control signals using the first termination adjustment logic; and

adjust the output impedance on the second port using the modified set of control signals.

19. (Original) The memory system of claim 18 wherein the first termination adjustment logic is further

adapted to at least one of selectively activate and de-activate one or more of a plurality of stacked transistor pairs included in the second resistive element using the modified set of control signals to adjust the output impedance on the second port.

20. (Original) The memory system of claim 18 further comprising second termination adjustment logic coupled to the second resistive element, and adapted to:

if the second termination adjustment logic is enabled, modify one or more secondary control signals; and

adjust the output impedance of the second port using the modified secondary control signals.

21. (Original) The memory system of claim 20 wherein the second termination adjustment logic is further adapted to at least one of selectively activate and de-activate one or more of a plurality of stacked transistor pairs included in a default device of the second resistive element using the modified secondary control signals to adjust the output impedance on the second port.